UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER OF PATENTS AND TRADEMARKS
Washington, D.C. 20231

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.
09/300,540	04/27/99	VAN GINNEKEN L	54355

MM91/0606

PILLSBURY MADISON & SUTRO LLP
1100 NEW YORK EAST TOWER
WASHINGTON DC 20005-3918

EXAMINER	
KIK,P	

ART UNIT	PAPER NUMBER
2825	

DATE MAILED: 06/06/01

Please find below and/or attached an Office communication concerning this application or proceeding.

Commissioner of Patents and Trademarks

Office Action Summary	Application No.	Applicant(s)	
	09/300,540	VAN GINNEKEN ET AL.	
	Examiner	Art Unit	
	Phallaka Kik	2825	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136 (a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____ .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) 1-30 is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) 1-30 is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claims _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are objected to by the Examiner.

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. § 119

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgement is made of a claim for domestic priority under 35 U.S.C. § 119(e).

Attachment(s)

15)☒ Notice of References Cited (PTO-892)
16)☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
17)☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) 5 and 6 .
18)☐ Interview Summary (PTO-413) Paper No(s). _____ .
19)☐ Notice of Informal Patent Application (PTO-152)
20)☐ Other:

DETAILED ACTION

Drawings

1. The drawings filed on 4/27/1997 are acceptable under the new rules as being easily readable and scannable.

Claim Rejections - 35 USC § 101

2. 35 U.S.C. 101 reads as follows:

> Whoever invents or discovers any new and useful process, machine, manufacture, or composition of matter, or any new and useful improvement thereof, may obtain a patent therefor, subject to the conditions and requirements of this title.

3. **Claims 21-30** are rejected under 35 U.S.C. 101 because the claimed invention is directed to non-statutory subject matter wherein the claims are directed to "data structures" representative of non-functional descriptive material since the descriptive material are merely stored so as to be read or outputted by a computer without creating any functional interrelationship, either as part of the stored data or as part of the computing processes performed by the computer, thus failing to impart functionality either to the data as so structured or to the computer (see *Warmerdam*, 33 F. 3rd at 1361, 31 USPQ2d at 1760).

Claim Rejections - 35 USC § 102

4. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless --

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

5. **Claims 1-6,14-20** are rejected under 35 U.S.C. 102(b) as being anticipated by **Rostoker et al.** (US Patent No. 5,541,849).

Rostoker et al. disclose a method and system for creating and validating low level description of electronic design from higher level behavior-oriented description, including estimation and comparison of timing parameters (abstract).

As per **claims 1-2,19-20**, all of the elements of the claims are illustrated in Fig. 9 (see also col. 9, line 60 to col. 12, line 22 and Fig. 12), wherein the electrical signals are generated by the VHDL compiler and simulator and design partitioner (blocks 904 and 908), logic synthesis is performed in blocks 912,916,910,918, and the physical placement is performed in blocks 920 and 922, and VHDL is a form of the hardware description language description, wherein the partitioning and composition steps (steps 3 and 5) provide for the retrieving a portion of the data model corresponding to the physical area while not retrieving portions of the data model not corresponding to the physical area and wherein the formal verification or validation (part of steps 3 and 6, col. 10, lines 10-21 and 34-54) must of necessity copy the data model to be used for formaly verification so that the original library models are not modified.

As per **claims 3-6,14-16**, the data model being a hierarchy of data objects having various objects attributes are described in col. 10, lines 4-28 (see also col. 15, line 48 to col. 17, line 5), wherein the objects having functional equivalents are inherently included as part of the

components in the library having the same function but different optimization criteria (i.e., higher speed or less area or more drive ability) as is common in the art.

As per **claims 17-18**, the common tool including a timing simulator is also described in col. 11, lines 47-55, 64 to col. 12, line 9.

6. **Claims 21-30** are rejected under 35 U.S.C. 102(b) as being anticipated by **Mahmood et al.** (US Patent No. 5,726,902).

Mahmood et al. disclose a method and apparatus for characterizing the timing behavior of datapath in integrated circuit design and fabrication, having an architecture library for representing digital circuits (abstract).

As per **claims 21-22,24-26**, all of the elements in the claims are taught in Table 1, Table 2 and Table 4 (see also col. 10, line 57 to col. 11, line 42; col. 11, line 8 to col. 12, line 43, and col. 13, line 66 to col. 14, line 61).

As per **claim 23**, the library including technology library and circuit library is also described in col. 16, lines 12-38.

As per **claim 27**, the plurality of cells having primitive cell and non-primitive cell is also described in col. 11, lines 31-42.

As per **claims 28-30**, since it is not clear from Applicant's specification what the KD tree data structure is, the tree expression as described in col. 6, line 46 to col. 7, line 26 meets these further limitations.

Claim Rejections - 35 USC § 103

7. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

8. **Claims 7-13** are rejected under 35 U.S.C. 103(a) as being unpatentable over **Rostoker et al.** (US Patent No. 5,541,849) in view of **Mahmood et al.** (US Patent No. 5,726,902).

As per **claims 7-13**, **Rostoker et al.** disclose all of the elements of claims 1 and 4 as discussed in the rejection of claims 1 and 4 above from which the claims depend but failed to specifically disclosed the KD tree data structured implementation. Such tree data structured is taught by **Mahmood et al.** used for optimally synthesizing an IC from HDL description (abstract; col. 6, line 46 to col. 7, line 26; col. 1, lines 50-62) wherein since it is not clear from Applicant's specification what the KD tree data structure is, the tree expression as described in col. 6, line 46 to col. 7, line 26 meets these further limitations. It would have been obvious to one of ordinary skilled in the art at the time of the invention to further incorporate the tree data structured implementation of the data model library as taught by **Mahmood et al.** to the method/system of **Rostoker et al.** because such tree data structured method optimally synthesize an IC from an HDL specification.

Conclusion

9. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

10. The following are other prior arts not relied upon but are considered pertinent to applicant's disclosure. Therefore, Applicants are requested to carefully consider them in response to this Office Action.

Aubel et al. (US Patent No. 5,696,693) disclose a method for placing logic functions and cells in a logic design using floor planning by analogy (abstract) wherein the logic functions are derived from the HDL file (col. 10, lines 1-32; Fig. 2) and the cell libraries includes hierarchy, graph tree structure (col. 2, lines 16-58).

Lemche et al. (US Patent No. 5,727,187) disclose a method of using logical names in post-synthesis electronic design automation systems (abstract) including tree structured library of components (col. 2, lines 25-60).

Iwasaki et al. (US Patent No. 5,623,417) disclose a method and apparatus for functional level data interface which permits the unification of functional design automation tools containing tree structured library components (Fig. 3; col. 4, lines 32-53).

Loos et al. (5,487,018) discloses an electronic design automation apparatus and method utilizing a physical information database for interfacing between a datapath cell library and a number of electronic design automation tools (e.g., datapath synthesis too, chip estimator, HDL generation tool, datapath compilation tool), wherein the database includes global parameters

applicable to every cell in the datapath cell library and local parameters defining attributes that are associated with individual cells in the datapath cell library (abstract; Fig. 2; col. 3, line 35 to col. 4, line 9).

Sharma et al. (US Patent 5,481,663) disclose a method and apparatus for designing circuit which uses parameterized Hardware Description Language (HDL) modules stored in a library, wherein a datapath synthesizer accesses the library and assigns values to parameters to form specific implementations of the parameterized HDL modules (abstract; Fig. 16).

Mahmood et al. (US Patent No. 5,519,627) disclose datapath synthesis method and apparatus utilizing a structured cell library (abstract; Fig. 4).

Dutt ("Generic component library characterization for high level synthesis", Proceedings of the Fourth CSI/IEEE International Symposium on VLSI Design, 1991, 4 January 1991, pp. 5-10) discloses a novel generator-generator language for the definition, generation, and maintenance of generic component description libraries used in high-level hardware synthesis wherein the every high-level synthesis system uses an implicit or explicit generic component library, wherein the library is hierarchically organized into types, generators, components, and instances, allowing the users to add and modify component types easily (abstract; pp. 6-9; Figure 1).

11. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Phallaka Kik whose telephone number is (703) 306-3039. The examiner can normally be reached on Monday to Thursday from 7:30 AM to 5 PM. The examiner can also be reached on alternate Fridays.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matthew S. Smith, can be reached at (703) 308-1323. The fax phone number for this Group is (703) 305-3431.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the Group receptionist whose telephone number is (703) 308-1782.

Any response to this action should be mailed to:

Commissioner of Patents and Trademarks

Washington, D.C. 20231

or faxed to:

(703) 305-3431, (for formal communications intended for entry)

Or:

(703) 308-5841 (for informal or draft communications, please label "PROPOSED" or "DRAFT" and let the examiner know prior to faxing)

Hand-delivered responses should be brought to Crystal Plaza 4, 2201 South Clark Place, Arlington, VA 22202, Fourth Floor (Receptionist).

PK

June 3, 2001

MATTHEW SMITH
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2800